CLAIMS

Please amend the following claims.

1. (Four Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an innermost side of the extension is adjacent to an outside surface of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

4. (Four Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate,

along the sidewalls of the recess, an innermost side of the extension is adjacent to an outside surface of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.